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CS 383

I pledge my honor that I have abided by the stevens honor system.

1. ALU stands for Arithmetic logic unit. CU stands for control unit. A register is a small part of the CPU that is for holding of data to be used by the processor. This data could be an instruction, memory address, bits, or characters. The purpose of the instruction register is to hold the instruction that is currently being executed by the processor.
2. A superscalar processor can make use of multiple execution units to run multiple instructions during a clock cycle.
3. Branch Delay spot to be executed immediately after the branch eliminates most of the branch delay. This imposes restrictions when debugging and managing breakpoints as special handling is needed.
4. Over time, the upgrade from 16 bit to 32 bit to 64-bit architecture has allowed CPUs to be able to address more and more memory. Now with 64 Bit, CPUs can address more than 4 GB of memory. CPUs have also become so much smaller in size as engineers continuously find out how to make the transistors they run on smaller. Currently, modern consumer CPUs are 14nm and 10nm is on the way. This allows for a lower profile less power consumption, which also over time has improved drastically. The creation of the multicore processor has driven speed and clock times significantly up as dual, quad, hexa and octa core processors become mainstream. Multiple cores allow for the CPU to execute multiple fetch cycles at time and process large amounts of information at once.
5. The problem with CPU design and Moore’s law is that even though engineers are consistently working on making CPU transistors smaller for smaller and faster processors, eventually due to the laws and nature of physics, it will become physically impossible to make smaller transistors and we will not be able to design smaller processors.

; Midterm.asm

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.include "m328Pdef.inc"

; Use r16 for X,

start:

ldi r16, 5

ldi r17 ,2

ldi r18, 3

ldi r19, 4

mul r16, r16

mov r20, r0

mul r20, r17

mov r21 ,r0

add r18, r19

mov r22, r0

sub r21, r22

mov r23, r0

jmp END

END: